

CS 631-01

Digital Design 2

2026-09-07

Combinational Logic
Sum-of-products

AND OR NOT

\Rightarrow \Rightarrow \Rightarrow

Today

Goal:

Implement a

4-bit counter

↙
4-bit adder + 4-bit register
clock

SR-Latch

Sub goal: N-bit Register

SR Latch

↓

Clock

↓

D Latch

↓

Multiplexor

↓

D Flip Flop

↓

D Flip Flop CLR EN

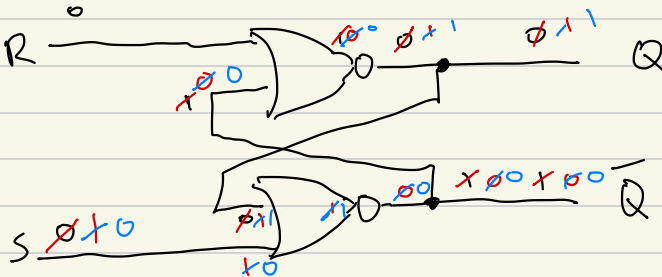
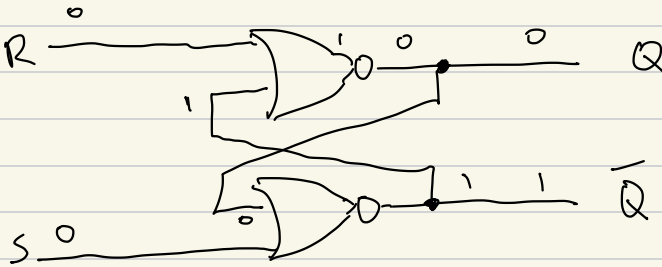
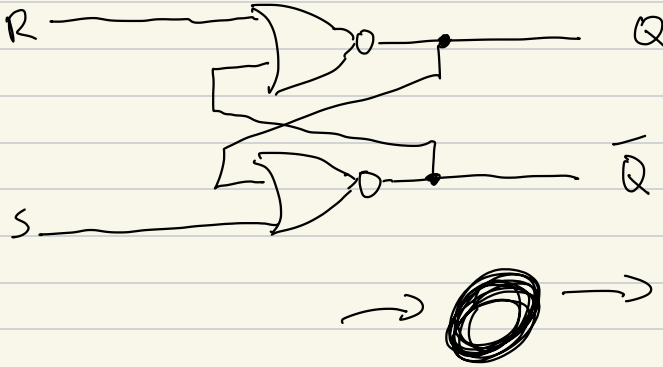
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N-bit Register

SQ Latch

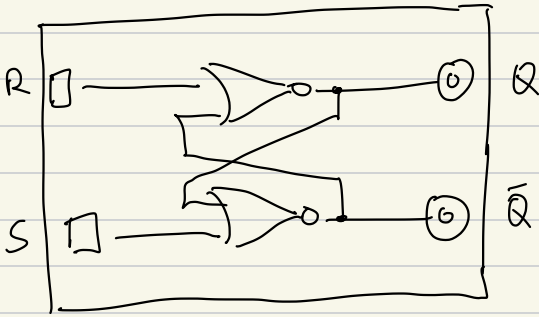
Set Reset

Static RAM

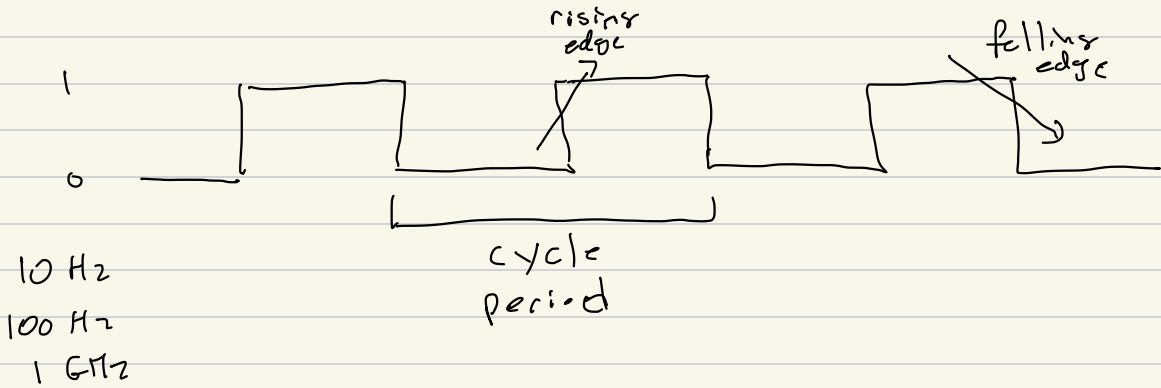


R	S	Q	Q̄
0	0	0	1
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
1	1	X	X

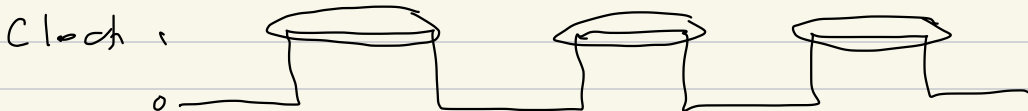
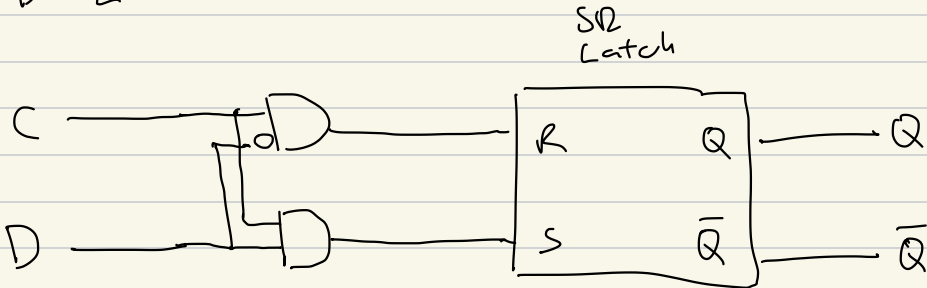
SQ Latch



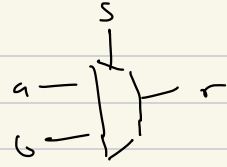
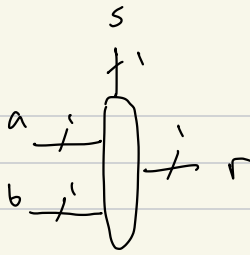
Clock (signal) crystal



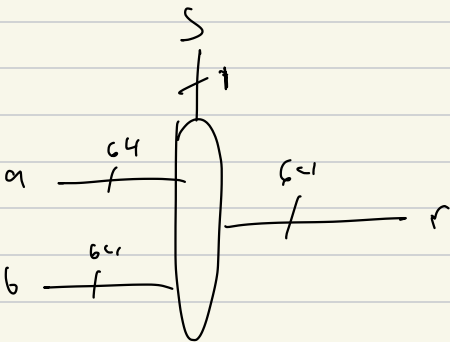
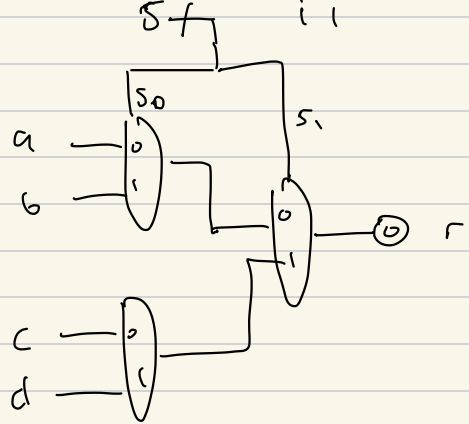
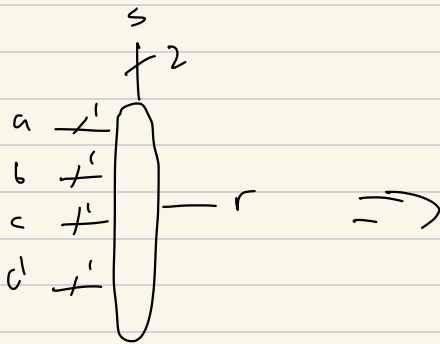
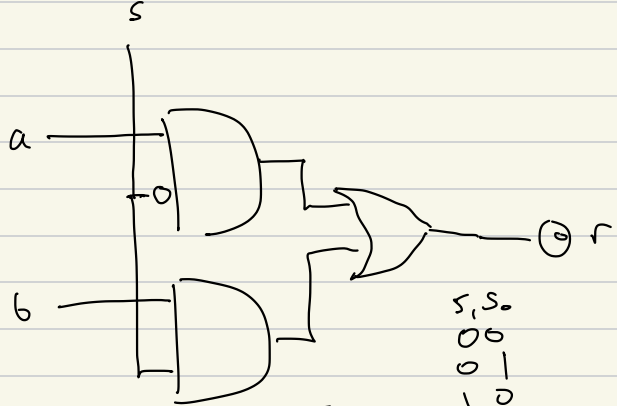
D Latch



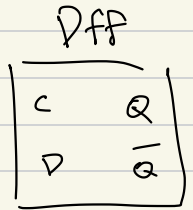
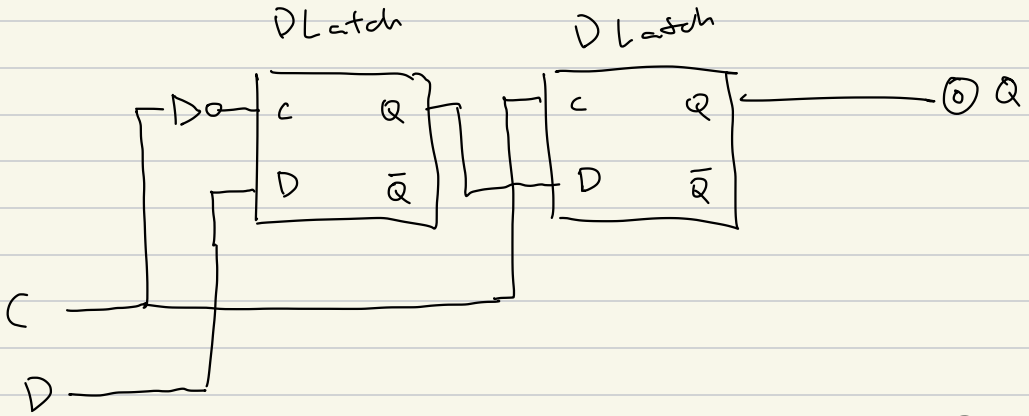
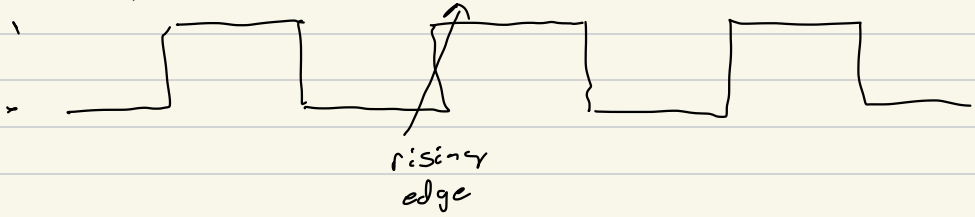
Multiplexor



a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



D Flip Flop



D Flip Flop with CLR and EN

